UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,395	09/24/2003	Yee-Chia Yeo	TSM03-0511	3960

43859 7590 04/06/2006

SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,395	YEO ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowability withdrawn

1. The indicated allowability of claims 24-47 and 58 are withdrawn in view of the reference(s) to Inaba. Rejections based on the reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 24-25, 33-36, 39-40, 45-52 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba, US patent No. 6,525,403.

Regarding claim 24, Inaba teaches (fig. 6) a method of forming a multiple-gate transistor, the method comprising: providing a bulk semiconductor substrate (11), forming a semiconductor fin (11a, substrate projection region) in the bulk semiconductor substrate, forming isolation regions (12) on sides of the semiconductor fin (11a), forming a gate dielectric (13) and a gate electrode (14) on a portion of the semiconductor fin, the gate electrode having a bottom surface (portion of the gate resting on 12), and forming a source region (15) and a drain region (16) in the semiconductor fin, the source region having a source-substrate junction (region where source region meets the substrate) and the drain region having a drain-substrate junction (region where drain region meets the substrate), the source-substrate junction or drain-substrate junction being higher than the bottom surface of the gate electrode.

Inaba does not disclose the process step of forming source/drain regions using a masking layer over the isolation region and covering a lower portion of the semiconductor fin; forming a source region and a drain region in uncovered portions of the semiconductor fin where the source-substrate or drain-substrate junction being higher than the bottom surface of the electrode by an amount based on the thickness of the masking layer.

However Inaba shows this missing step with respect to his acknowledged prior art of figure 5. Specifically figure 5 shows a masking layer (123) over the isolation region and covering a lower portion of the semiconductor fin; and forming a source and drain region in uncovered portions of the semiconductor fin, the source region having a source-substrate junction and the drain region having a drain substrate junction, the source-substrate junction or drain-substrate junction being higher than the bottom surface of the electrode by an amount based on the thickness of the masking layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of the mask layer as taught in the prior art of Inaba in the structure of embodiment of fig. 6 in order to improve the heat conductivity and minimize current degradation caused by heat due to Joule effect (col. 6, lines 9-15). The combined process of embodiments of figs 4-6 teaches forming a masking layer over the isolation region and covering a lower portion of the semiconductor fin; and forming a source and drain region in uncovered portions of the semiconductor fin, the source region having a source-substrate junction and the drain region having a drain substrate junction, the source-substrate junction or drain-substrate junction being higher

than the bottom surface of the electrode by an amount based on the thickness of the masking layer.

Regarding claims 25 and 58, Inaba does not explicitly teach that the source-substrate junction and drain-substrate junction is higher than the bottom surface of the gate electrode by at least 50 and a distance of between about 50 and 500 angstroms o.

Parameters such as height and distance in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during device fabrication.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the source-substrate junction and drain-substrate junction as claimed in order to improve the heat conductivity and minimize current degradation caused by heat due to Joule effect (col. 6, lines 9-15).

Regarding claim 33, Inaba teaches substantially the entire claimed process of claim 24 above including the semiconductor fin comprises silicon (col. 4, lines 16-29).

Regarding claim 35, Inaba teaches substantially the entire claimed process of claim 24 above including the gate dielectric (13) is silicon oxide (col. 4, lines 29-33).

Regarding claim 36, Inaba teaches substantially the entire claimed process of claim 24 above including the gate dielectric comprises a high permittivity material. Inaba teaches the gate dielectric material to be silicon oxide. Since silicon oxide has a high permittivity compared to for example to a metal, Inaba inherently teaches a high permittivity material.

Regarding claim 39, Inaba teaches substantially the entire claimed method of claim 24 above except explicitly stating that tie dielectric layer is between about 3 and about 100 angstroms.

Parameters such as height and thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during device fabrication.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the dielectric layer as claimed in order to improve the heat conductivity and minimize current degradation caused by heat due to Joule elect.

Regarding claim 40, Inaba teaches substantially the entire claimed process of claim 24 above including the gate electrode is polycrystalline silicon (col. 7, lines 45-49).

Regarding claims 45 and 46, Inaba teaches (fig. 6) substantially the entire claimed process of claim 24 above including the multiple gate transistors is a double gate transistor and a triple gate transistor.

Regarding claim 47, Inaba teaches substantially the entire claimed process of claim 24 above including the multiple gate transistors is an omega-gate transistor (fig. 6).

Regarding claim 48, Inaba teaches (fig. 6) a method of forming a semiconductor device, the method comprising: providing a silicon substrate (11); etching portions of the silicon substrate to form at least one semiconductor fin (substrate projection region, 11a); forming a gate dielectric layer (13) over the semiconductor fin (11a); forming a

gate electrode (14) layer over the gate dielectric layer; etching portions of the gate electrode layer to form a gate electrode, the gate electrode overlying sidewalls and a top surface of the semiconductor fin (refer to figs. 6 and 9); and doping the sidewall of the semiconductor fin above the region of material (also refer col. 8, lines 58-67 and col. 9, lines 1-12).

Inaba does not disclose the process step of forming a region of material adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface of the region of material.

However Inaba shows this missing step with respect to his acknowledged prior art of figure 5. Specifically figure 5 shows a masking layer/region of material (123) adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface of the region of material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of the mask layer/region of material taught in the prior art of Inaba in the structure of embodiment of fig. 6 in order to improve the heat conductivity and minimize current degradation caused by heat due to Joule effect (col. 6, lines 9-15). The combined process of embodiments of figs 4-6 teaches forming a masking layer/region of material adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface of the region of material. In addition it would have been obvious to remove the masking layers after source/drain implantation.

Regarding claim 49, Inaba teaches (fig. 6) substantially the entire claimed process of claim 48 above including forming the isolation region (12) being formed after etching portions of the silicon substrate but before forming the gate dielectric (col. 4, lines 16-33).

Regarding claim 50, Inaba teaches substantially the entire claimed process of claim 48 above including forming a masking material over the silicon substrate and wherein the step of etching portions of the silicon substrate is performed in alignment with the masking material (col. 8, lines 58-67 and col. 9, lines 1-12).

Regarding claim 51, Inaba teaches substantially the entire claimed process of claim 48 above including removing the masking material after the semiconductor fin is formed (col. 9, lines 1-12).

Regarding claim 52, Inaba teaches substantially the entire claimed process of claim 48 above including the gate dielectric layer and the gate electrode layer are formed over the masking material (col. 8, lines 58-67 and col. 9, lines 1-12).

Regarding claims 53, Inaba teaches substantially the entire claimed method of claim 48 above including depositing a dielectric layer or depositing an oxide material (123) (refer to fig. 5).

Regarding claim 55, Inaba teaches substantially the entire claimed process of claim 48 above including forming an isolation region (12) adjacent the semiconductor region.

Regarding claim 57, Inaba teaches the entire claimed process of claims 48 and 49 above including depositing an oxide material (col. 11, lines 37-40).

4. Claims 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba in view of Park et al. (A 40nm body-tied Finfet (OMEGA MOSFET) using bulk Si wafer, Physica E 19 (2003), pages 6-12).

Regarding claim 26, Inaba teaches substantially the entire claimed method of claim 24 above except explicitly stating forming a mask over the bulk semiconductor substrate, and etching exposed regions of the semiconductor substrate to form the semiconductor fin.

Park teaches (refer to device fabrication section and figs. 5a-5h) performing photolithography process on a bulk semiconductor substrate to form a fin structure (fig. 5(e)) using different masking layers.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the photolithographic process taught by Park in the method of Inaba in order to scale down the device size.

Regarding claim 27, Inaba teaches substantially the entire claimed method of claim 24 above including removing the mask (fig. 5(e)).

Regarding claim 28, Inaba teaches substantially the entire claimed method of claim 24 above including the mask comprises a photoresist.

Since the combined process of Inaba and Park teaches photolithographic process, it inherently teaches a mask layer comprising photoresist.

Regarding claim 29, Inaba teaches substantially the entire claimed process of claim 24 above including a silicon oxide as a mask layer (Park, page 8, 2nd col. 1st paragraph).

Regarding claim 30, Inaba teaches substantially the entire claimed method of claim 24 above including strapping the source and drain regions with a conductive material (Park, page 9).

Regarding claim 31, Inaba teaches substantially the entire claimed method of claim 24 above including forming spacers on sides of the gate electrode (park, page 9, 1st, paragraph)

5. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba in view of Huang US patent No. 5,893,741.

Inaba teaches substantially the entire claimed method of claim 24 above except explicitly stating performing selective epitaxy on the source and drain regions.

Huang teaches forming source and drain regions using selective epitaxial growth in the process of forming FET structure (col. 1, lines 29-40).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the selective epitaxial process taught by Huang in the process of Inaba in order to over come problems associated with growing silicon on doped surfaces.

6. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba in view of Clark et al. 6,635,909.

Regarding claim 34, Inaba teaches substantially the entire claimed method of claim 24 above except explicitly stating that the fin comprises silicon and germanium.

Clark teaches a fin FET structure where the fin is formed of silicon/germanium layer in the process of forming a strained fin FET device.

It would have been obvious to one of ordinary skill in the art at the time invention was made to substitute the fin layer in the process of Inaba with silicon/germanium as taught by Clark in order to improve carrier mobility that is gained due to the strained silicon/germanium layer.

7. Claims 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba in view of Yu US patent No. 6,342,410.

Regarding claims 37-38, Inaba teaches substantially the entire claimed method of claim 24 above except explicitly stating that the gate dielectric comprises a material selected from the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and zirconium oxide, and combinations thereof or the gate dielectric comprises a material with a relative permittivity greater than about 5.

Yu teaches the use of high permittivity gate dielectric material such as aluminum oxide with a dielectric constant of 8 in the process of forming a field effect transistor (col. 4, lines 36-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the high permittivity material taught by Yu in the process of Inaba in order to minimize charge carrier tunneling through the gate dielectric.

8. Claims 41and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba in view of Yu US patent No. 6,475,890.

Inaba teaches substantially the entire claimed method of claim 24 above except explicitly stating that the gate electrode comprises poly-SiGe or metal.

Yu teaches forming gate material using poly-SiGe or various metals in the process of forming FET device (col. 6, lines 13-21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the gate materials suggested by Yu in the process of Inaba in order to form fin transistor with improved gate conductivity.

9. Claims 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba in view of Hu et al. US patent No. 6,413,802.

Inaba teaches substantially the entire claimed method of claim 24 above except explicitly stating that the gate electrode comprises a metallic nitride.

Hu teaches forming a gate material using titanium nitride in the process of forming a fin FET transistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the gate material suggested by Hu in the process of Inaba in order to adjust the work function the gate.

10. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba in view of Muller et al. US patent No. 6,432,829.

Inaba teaches substantially the entire claimed process of claim 24 above except explicitly stating that the gate electrode comprises a metallic silicide.

Muller teaches coating the gates with a silicide layer in the process of forming fin device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the silicide layer taught by Muller in the process of Inaba in order to adjust the work function of the gates.

11. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba, in view of Yu US patent No. 6,342,410.

Inaba teaches substantially the entire claimed method of claim 48 above except explicitly stating that the gate dielectric comprises a material with a relative permittivity greater than about 5.

Yu teaches the use of high permittivity gate dielectric material such as aluminum oxide with a dielectric constant of 8 in the process of forming a field effect transistor (col. 4, lines 36-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the permittivity material taught by Yu in the process of Inaba in order to minimize charge carrier tunneling through the gate dielectric.

12. Claim 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba, in view of Park.

Inaba teaches substantially the entire claimed process of claim 48 above except explicitly stating removing region of material after doping.

Forming and removing of a masking layer is conventional and also taught by Park (figs. 5a-5e), in the process of forming a body-tied finfet structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of removing the masking layer after a doping process in order to protect the body region.

Affidavit

13. The affidavit filed on 5/16/2005 is not found to be persuasive since the statement therein is not supported by the disclosure of Inaba, that is figures 6-10 clearly shows a space between the lower end of the source/drain region and the top surface of the layer (12), which corresponds to the bottom surface of the gate electrode.

Response to Arguments

14. Applicant's arguments filed 1/6/2006 have been fully considered but they moot in view of new grounds of rejection.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
March 29, 2006

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800